

NSBC114EDP6T5G Series

Preferred Devices

Dual Digital Transistors (BRT)

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The digital transistor contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The digital transistor eliminates these individual components by integrating them into a single device. The use of a digital transistor can reduce both system cost and board space. The device is housed in the SOT-963 package which is designed for low power surface mount applications.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- The SOT-963 Package can be Soldered using Wave or Reflow.
- Available in 4 mm, 8000 Unit Tape & Reel
- These are Pb-Free Devices
- These are Halide-Free Devices

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

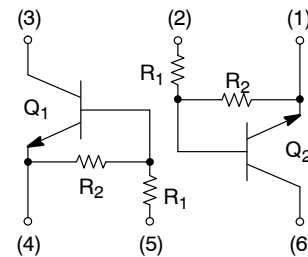
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



ON Semiconductor®

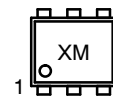
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NPN SILICON DIGITAL TRANSISTORS



SOT-963
CASE 527AD

MARKING DIAGRAM



- X = Specific Device Code
- M = Date Code
- = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NSBC114EDP6T5G	SOT-963 (Pb-Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DEVICE MARKING INFORMATION

See specific marking information in the device marking table on page 2 of this data sheet.

NSBC114EDP6T5G Series

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
SINGLE HEATED			
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 1) Derate above 25°C	P_D	231 1.9	mW mW/ $^\circ\text{C}$
Thermal Resistance (Note 1) Junction-to-Ambient	$R_{\theta JA}$	540	$^\circ\text{C}/\text{W}$
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 2) Derate above 25°C	P_D	269 2.2	mW mW/ $^\circ\text{C}$
Thermal Resistance (Note 2) Junction-to-Ambient	$R_{\theta JA}$	464	$^\circ\text{C}/\text{W}$
DUAL HEATED (Note 3)			
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 1) Derate above 25°C	P_D	339 2.7	mW mW/ $^\circ\text{C}$
Thermal Resistance (Note 1) Junction-to-Ambient	$R_{\theta JA}$	369	$^\circ\text{C}/\text{W}$
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 2) Derate above 25°C	P_D	408 3.3	mW mW/ $^\circ\text{C}$
Thermal Resistance (Note 2) Junction-to-Ambient	$R_{\theta JA}$	306	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

1. FR-4 @ 100 mm², 1 oz. copper traces, still air.
2. FR-4 @ 500 mm², 1 oz. copper traces, still air.
3. Dual heated values assume total power is sum of two equally powered channels.

DEVICE MARKING AND RESISTOR VALUES

Device	Marking*	R1 (k)	R2 (k)	Package	Shipping†
NSBC114EDP6T5G	A (270°)	10	10	SOT-963 (Pb-Free)	8000/Tape & Reel
NSBC124EDP6T5G	R (0°)	22	22		
NSBC144EDP6T5G	D (0°)	47	47		
NSBC114YDP6T5G	P (0°)	10	47		
NSBC123TDP6T5G	A (90°)	2.2	∞		
NSBC143EDP6T5G	T (0°)	4.7	4.7		
NSBC143ZDP6T5G	Y (0°)	4.7	47		
NSBC123JDP6T5G	D (90°)	2.2	47		
NSBC144WDP6T5G	V (0°)	47	22		
NSBC114TDP6T5G	R (180°)	10	∞		
NSBC115TDP6T5G	F (0°)	100	∞		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*(XX°) = Degree rotation in the clockwise direction.

NSBC114EDP6T5G Series

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Base Cutoff Current ($V_{CB} = 50\text{ V}$, $I_E = 0$)	I_{CBO}	–	–	100	nAdc
Collector–Emitter Cutoff Current ($V_{CE} = 50\text{ V}$, $I_B = 0$)	I_{CEO}	–	–	500	nAdc
Emitter–Base Cutoff Current ($V_{EB} = 6.0\text{ V}$, $I_C = 0$)	I_{EBO}	–	–	0.5	mAdc
NSBC114EDP6T5G		–	–	0.2	
NSBC124EDP6T5G		–	–	0.1	
NSBC144EDP6T5G		–	–	0.2	
NSBC114YDP6T5G		–	–	0.9	
NSBC114TDP6T5G		–	–	4.0	
NSBC123TDP6T5G		–	–	0.1	
NSBC115TDP6T5G		–	–	1.5	
NSBC143EDP6T5G		–	–	0.18	
NSBC143ZDP6T5G		–	–	0.2	
NSBC123JDP6T5G		–	–	0.13	
NSBC144WDP6T5G		–	–		
Collector–Base Breakdown Voltage ($I_C = 10\ \mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	50	–	–	Vdc
Collector–Emitter Breakdown Voltage (Note 4) ($I_C = 2.0\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	50	–	–	Vdc
ON CHARACTERISTICS (Note 4)					
DC Current Gain ($V_{CE} = 10\text{ V}$, $I_C = 5.0\text{ mA}$)	h_{FE}	35	60	–	
NSBC114EDP6T5G		60	100	–	
NSBC124EDP6T5G		80	140	–	
NSBC144EDP6T5G		80	140	–	
NSBC114YDP6T5G		160	350	–	
NSBC114TDP6T5G/NSBC115TDP6T5G		15	30	–	
NSBC143EDP6T5G		80	200	–	
NSBC143ZDP6T5G		80	150	–	
NSBC123JDP6T5G		80	140	–	
NSBC144WDP6T5G		80	140	–	
Collector–Emitter Saturation Voltage ($I_C = 10\text{ mA}$, $I_B = 0.3\text{ mA}$)	$V_{CE(sat)}$	–	–	0.25	Vdc
NSBC114EDP6T5G/NSBC124EDP6T5G					
NSBC144EDP6T5G/NSBC114YDP6T5G					
NSBC123JDP6T5G/NSBC144WDP6T5G					
($I_C = 10\text{ mA}$, $I_B = 1\text{ mA}$)					
NSBC143EDP6T5G/NSBC143ZDP6T5G					
NSBC114TDP6T5G/NSBC123TDP6T5G					
($I_C = 10\text{ mA}$, $I_B = 5.0\text{ mA}$)					
NSBC115TDP6T5G					
Output Voltage (on) ($V_{CC} = 5.0\text{ V}$, $V_B = 2.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	V_{OL}	–	–	0.2	Vdc
NSBC114TDP6T5G		–	–	0.2	
NSBC114EDP6T5G		–	–	0.2	
NSBC124EDP6T5G		–	–	0.2	
NSBC114YDP6T5G		–	–	0.2	
NSBC123TDP6T5G		–	–	0.2	
NSBC143EDP6T5G		–	–	0.2	
NSBC143ZDP6T5G		–	–	0.2	
NSBC123JDP6T5G		–	–	0.2	
($V_{CC} = 5.0\text{ V}$, $V_B = 3.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)					
NSBC144EDP6T5G		–	–	0.2	
($V_{CC} = 5.0\text{ V}$, $V_B = 4.0\text{ V}$, $R_L = 1.0\text{ k}\Omega$)					
NSBC144WDP6T5G		–	–	0.2	
($V_{CC} = 5.0\text{ V}$, $V_B = 5.0\text{ V}$, $R_L = 1.0\text{ k}\Omega$)					
NSBC115TDP6T5G		–	–	0.2	

4. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%.

NSBC114EDP6T5G Series

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 5)					
Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (off) ($V_{CC} = 5.0\text{ V}$, $V_B = 0.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$) NSBC114EDP6T5G/NSBC124EDP6T5G NSBC144EDP6T5G/NSBC114YDP6T5G NSBC143EDP6T5G/NSBC123JDP6T5G NSBC144WDP6T5G ($V_{CC} = 5.0\text{ V}$, $V_B = 0.25\text{ V}$, $R_L = 1.0\text{ k}\Omega$) NSBC123TDP6T5G/NSBC143ZDP6T5G/NSBC114TDP6T5G/ NSBC115TDP6T5G	V_{OH}	4.9	–	–	Vdc
Input Resistor	R1	7.0 7.0 15.4 32.9 7.0 7.0 1.5 3.3 3.3 1.54 32.9 70	10 10 22 47 10 10 2.2 4.7 4.7 2.2 47 100	13 13 28.6 61.1 13 13 2.9 6.1 6.1 2.86 61.1 130	k Ω
Resistor Ratio	R_1/R_2	0.8 0.17 – 0.055 0.038 1.7	1.0 0.21 – 0.1 0.047 2.1	1.2 0.25 – 0.185 0.056 2.6	

5. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%.

NSBC114EDP6T5G Series

TYPICAL ELECTRICAL CHARACTERISTICS – NSBC114EDP6T5G

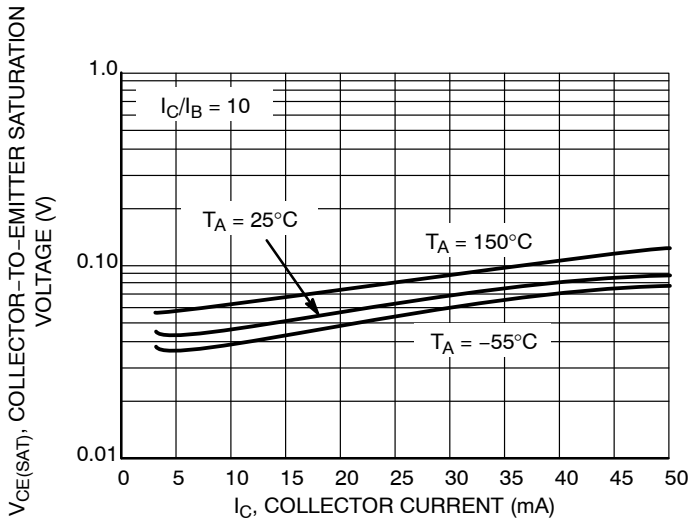


Figure 1. $V_{CE(sat)}$ vs. I_C

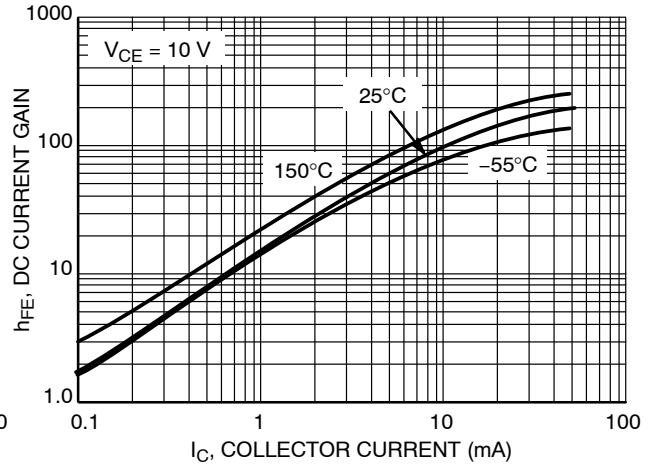


Figure 2. DC Current Gain

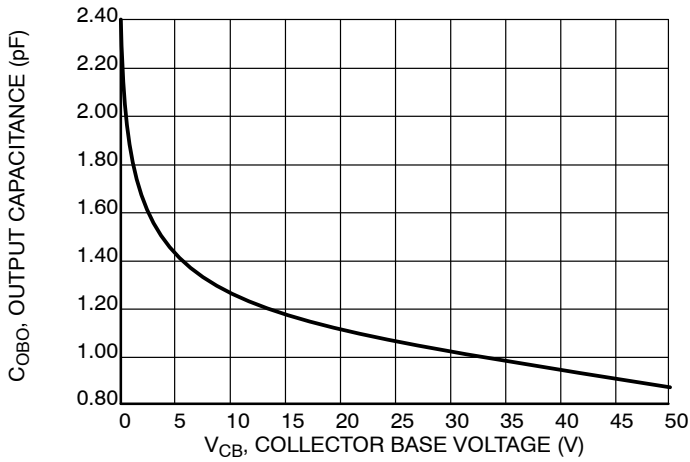


Figure 3. Output Capacitance

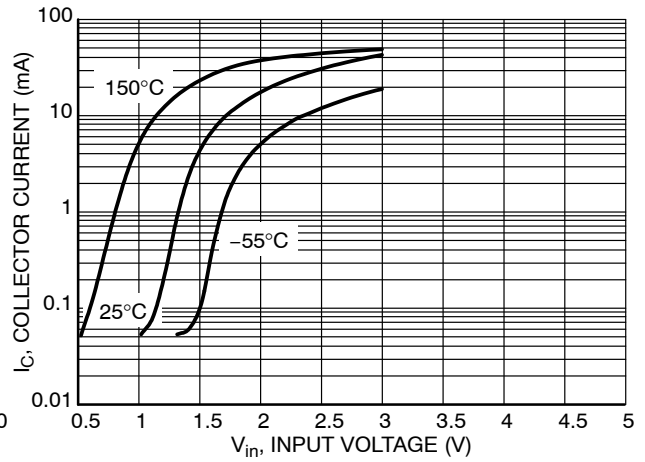


Figure 4. Output Current vs. Input Voltage

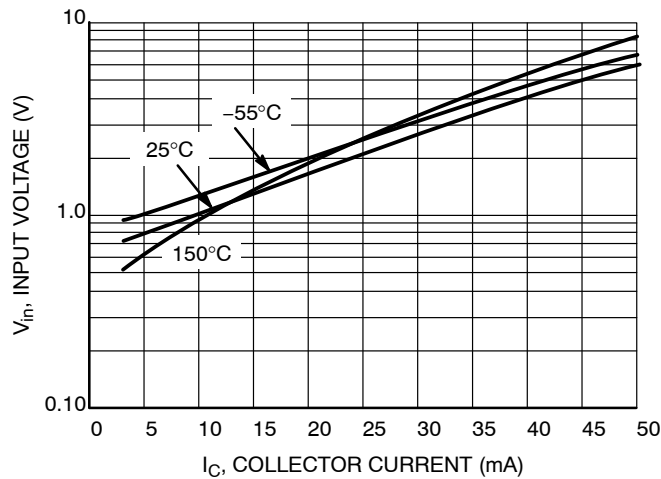


Figure 5. Input Voltage vs. Output Current

NSBC114EDP6T5G Series

TYPICAL APPLICATIONS FOR NPN BRTs

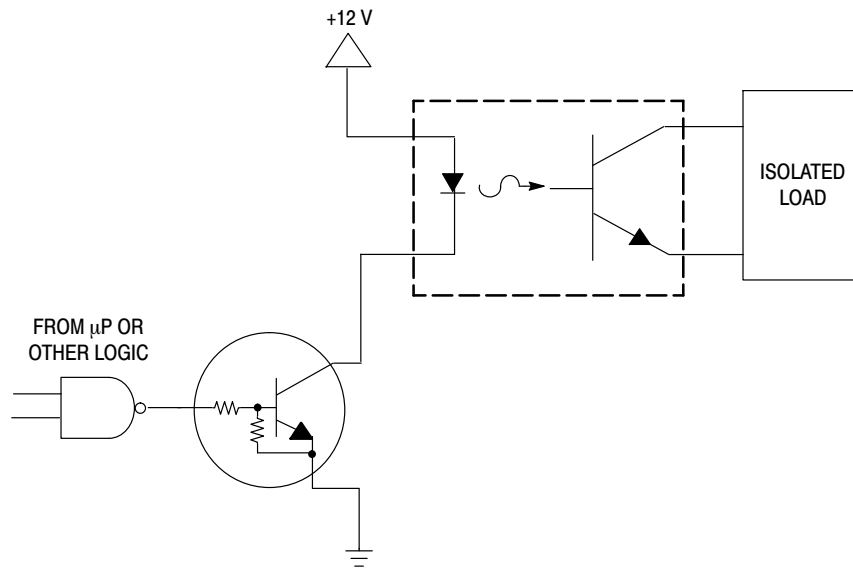


Figure 6. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

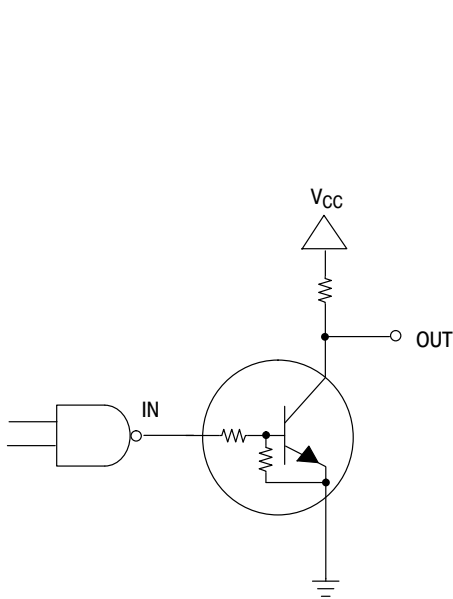


Figure 7. Open Collector Inverter: Inverts the Input Signal

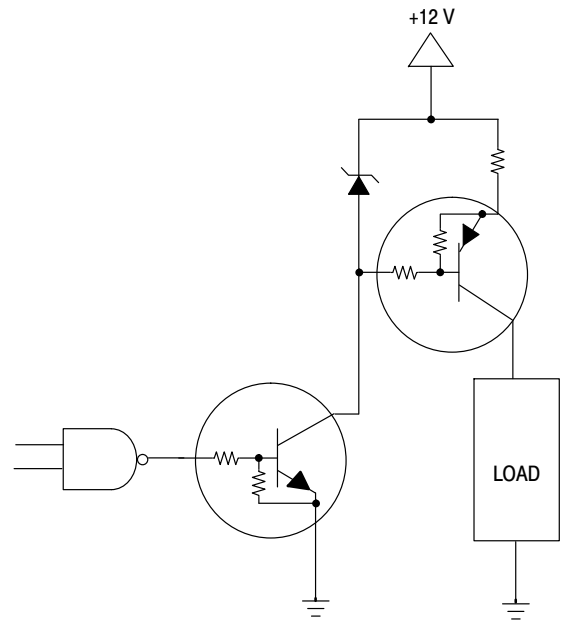
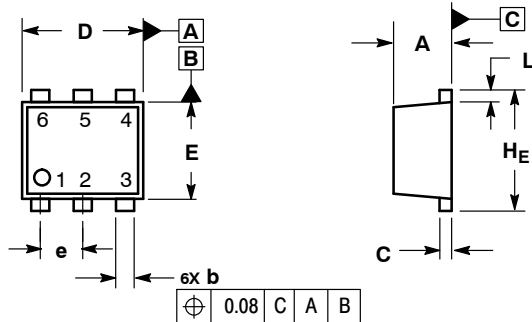


Figure 8. Inexpensive, Unregulated Current Source

NSBC114EDP6T5G Series

PACKAGE DIMENSIONS

SOT-963
CASE 527AD-01
ISSUE D

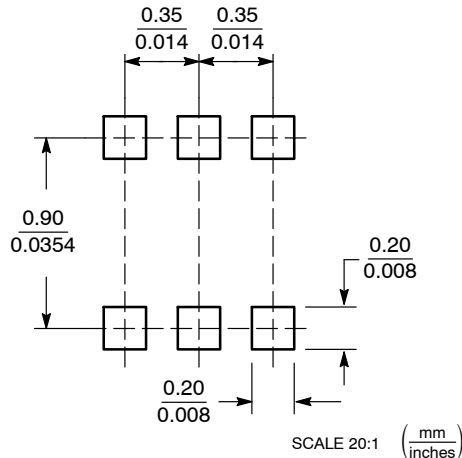


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.34	0.37	0.40			
b	0.10	0.15	0.20	0.004	0.006	0.008
C	0.07	0.12	0.17	0.003	0.005	0.007
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.75	0.80	0.85	0.03	0.032	0.034
e	0.35 BSC			0.014 BSC		
L	0.05	0.10	0.15	0.002	0.004	0.006
HE	0.95	1.00	1.05	0.037	0.039	0.041

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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